What is Claimed Is:

1. A rail-to-rail operational amplifier circuit to extract a true mean of two signals, comprising:

an n-type buffer input stage that receives the two signals and produces a first offset common mode output signal therefrom;

an n-type amplifier input stage that receives both the first offset common mode output signal and a first feedback signal, and produces a first differential error signal therefrom;

a p-type buffer input stage that receives the two signals and produces a second offset common mode signal therefrom;

a p-type amplifier input stage that receives both the second offset common mode output signal and a second feedback signal, and produces a second differential error signal therefrom;

a differential input high-gain amplifier output stage that receives the first and second differential error signals and produces a true common mode output signal that is substantially equal to the true mean of the two signals;

a feedback stage that receives the true common mode output signal and produces the first and second feedback signals therefrom; and

a transitioning stage that controls how much the first differential error signal from the n-type amplifier input stage and the second differential signal from the p-type amplifier input stage contribute to the differential input of the high-gain amplifier output stage.

2. The circuit of claim 1, wherein the two signals comprise a differential signal.

3. The circuit of claim 1, wherein feedback stage comprises a matched buffer stage.

4. The circuit of claim 1, wherein the transitioning circuit controls how a drive current is split between the n-type amplifier input stage and the p-type amplifier input stage.

5. The circuit of claim 4, wherein:

a first portion of the drive current is provided to the n-type amplifier input stage and effects a magnitude of the first differential error signal; and

a second portion of the drive current is provided to the p-type amplifier input stage and effects a magnitude of the second differential error signal.

6. The circuit of claim 5, wherein the first and second differential error signals are added at the differential input of the high-gain amplifier output stage.

7. The circuit of claim 6, wherein the n-type buffer input stage (202n) includes:

a first n-type transistor (Qn1) having a base forming a first input, a collector connected to a high rail potential, and having an emitter;

a first current source connecting the emitter of the first n-type transistor (Qn1) to a low rail potential;

a second n-type transistor (Qn2) having a base forming a second input, a collector connected to the high rail potential, and having an emitter;

a second current source connecting the emitter of the second n-type transistor (Qn2) to the low rail potential; and

a first pair of resistors connected in series between the emitter of the first n-type transistor (Qn1) and the emitter of the second n-type transistor (Qn2);

wherein the first offset common mode output signal is produced between the pair of resistors.

8. The circuit of claim 7, wherein the p-type amplifier input stage (202p) includes:

a first p-type transistor (Qp1) having a base connected to the base of the first n-type transistor (Qn1), a collector connected to the low rail potential, and having an emitter;

a third current source connecting the emitter of the first p-type (Qp1) transistor to the high rail potential;

a second p-type transistor (Qp2) having a base connected to the base of the second n-type transistor (Qn2), a collector connected to the low rail potential, and having an emitter;

a fourth current source connecting the emitter of the second p-type transistor (Qp2) to the high rail potential; and

a second pair of resistors connected in series between the emitter of the first p-type transistor (Qp1) and the emitter of the second p-type transistor (Qp2);

wherein the second offset common mode output signal is produced between the pair of resistors.

9. The circuit of claim 8, wherein the n-type amplifier input stage (204n) includes:

a third n-type transistor (Qn3) having a base connected between the first pair of resistors, a collector, and an emitter;

a fourth n-type transistor (Qn4) having an emitter connected to the emitter of the third n-type transistor (Qn3), and having a base and a collector;

a fifth current source connecting the collector of the third n-type transistor (Qn3) to the high rail potential;

a sixth current source connecting the collector of the fourth n-type transistor (Qn4) to the high rail potential;

wherein the base of the third n-type transistor (Qn3) receives the first offset common mode output signal;

wherein the base of the fourth n-type transistor (Qn4) receives the first feedback signal; and

wherein the emitters of the third and forth n-type transistors (Qn3 and Qn4) receive the first portion of the drive current; and

wherein the collectors of the third and forth n-type transistors (Qn3 and Qn4) provide the differential error signal.

10. The circuit of claim 9, wherein the p-type amplifier input stage (204p) includes:

a third p-type transistor (Qp3) having a base connected between the second pair of resistors, a collector, and an emitter;

a fourth p-type transistor (Qp4) having an emitter connected to the emitter of the third n-type transistor (Qn3), and having a base and a collector;

a seventh current source connecting the collector of the third p-type transistor (Qp3) to the low rail potential;

an eighth current source connecting the collector of the fourth p-type transistor (Qp4) to the low rail potential;

wherein the base of the third p-type transistor (Qp3) receives the second offset common mode output signal;

wherein the base of the fourth p-type transistor (Qn4) receives the second feedback signal;

wherein the emitters of the third and forth p-type transistors (Qp3 and Qp4) receive the second portion of the drive current; and

wherein the collectors of the third and forth p-type transistors (Qp3 and Qp4) provide the second differential error signal.

11. The circuit of claim 10, wherein the transitioning circuit includes:

a reference transistor (Qref) having a base receiving a reference voltage, an emitter connected to the emitters of the third and fourth n-type transistors (Qn3 and Qn4), and having a collector; and

a current mirror having an input connected to the collector of the reference transistor (Qref) and an output of the current mirror providing the second portion of the drive current to the emitters of the third and fourth p-type transistors (Qp3 and Qp4).

12. The circuit of claim 1, wherein:

the n-type stages include npn transistors; and

the p-type stages include pnp transistors.

13. The circuit of claim 1, wherein:

the n-type stages include NMOS transistors; and

the p-type stages include PMOS transistors.

14. A rail-to-rail operational amplifier to extract a true mean of two signals, comprising:

first and second buffer input stages, each adapted to receive the two signals;

a first amplifier input stage, coupled to an output of the first buffer input stage, and adapted to operate when a mean of the two signals is near an upper rail voltage;

a second amplifier input stage, coupled to an output of the second buffer input stage, and adapted to operate when the mean of the two signals is near a lower rail voltage; and

a transitioning stage adapted to control how much each of the first and the second amplifier input stages contributes to an input of a high-gain amplifier output stage, when a mean of the two signals is between the upper and lower rail voltages; and

a feedback stage adapted to feed an output of the high-gain amplifier output stage back to the first and second amplifier input stages.

15. The amplifier of claim 14, wherein the two signals comprise a differential signal.

16. A rail-to-rail operational amplifier circuit to extract a true mean of two signals, comprising:

an n-type buffer input stage that receives the two signals and produces a first offset common mode output signal therefrom;

an n-type amplifier input stage that receives both the first offset common mode output signal and a first feedback signal, and provides a first differential error signal to a differential input of a high-gain amplifier output stage;

a p-type buffer input stage that receives the two signals and produces a second offset common mode signal therefrom;

a p-type amplifier input stage that receives both the second offset common mode output signal and a second feedback signal, and provides a second differential error signal to the differential input of the high-gain amplifier output stage;

a feedback stage that receives a true common mode output signal from the high-gain amplifier output stage and provides the first and second feedback signals, respectively, to the n-type and p-type amplifier input stages; and

a transitioning stage that controls magnitudes of the first and second differential error signals.

17. The circuit of claim 16, wherein:

the n-type stages include npn transistors; and

the p-type stages include pnp transistors.

18. The circuit of claim 16, wherein:

the n-type stages include NMOS transistors; and

the p-type stages include PMOS transistors.